

# PDTB113E series

PNP 500 mA, 50 V resistor-equipped transistors;  
R1 = 1 k $\Omega$ , R2 = 1 k $\Omega$

Rev. 01 — 27 April 2005

Product data sheet

## 1. Product profile

### 1.1 General description

500 mA PNP Resistor-Equipped Transistors (RET) family.

Table 1: Product overview

Type number	Package			NPN complement
	Philips	JEITA	JEDEC	
PDTB113EK	SOT346	SC-59A	TO-236	PDTD113EK
PDTB113ES <a href="#">[1]</a>	SOT54	SC-43A	TO-92	PDTD113ES
PDTB113ET	SOT23	-	TO-236AB	PDTD113ET

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#)).

### 1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- 500 mA output current capability
- Reduces component count
- Reduces pick and place costs
- $\pm 10$  % resistor ratio tolerance

### 1.3 Applications

- Digital application in automotive and industrial segments
- Controlling IC inputs
- Cost-saving alternative for BC807 series in digital applications
- Switching loads

### 1.4 Quick reference data

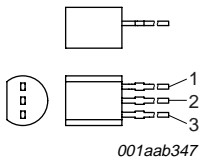
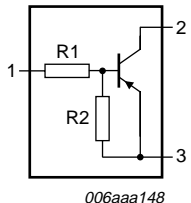
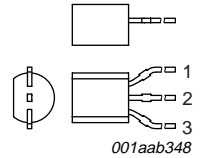
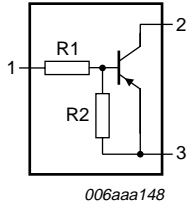
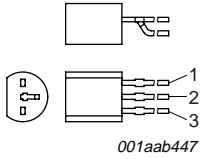
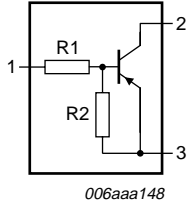
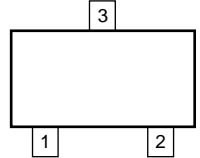
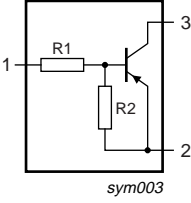
Table 2: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V
I <sub>O</sub>	output current (DC)		-	-	-500	mA
R1	bias resistor 1 (input)		0.7	1.0	1.3	k $\Omega$
R2/R1	bias resistor ratio		0.9	1.0	1.1	

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## 2. Pinning information

Table 3: Pinning

Pin	Description	Simplified outline	Symbol
<b>SOT54</b>			
1	input (base)	 <p>001aab347</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54A</b>			
1	input (base)	 <p>001aab348</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54 variant</b>			
1	input (base)	 <p>001aab447</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT23, SOT346</b>			
1	input (base)	 <p>006aaa144</p>	 <p>sym003</p>
2	GND (emitter)		
3	output (collector)		

### 3. Ordering information

Table 4: Ordering information

Type number	Package		
	Name	Description	Version
PDTB113EK	SC-59A	plastic surface mounted package; 3 leads	SOT346
PDTB113ES <sup>[1]</sup>	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTB113ET	-	plastic surface mounted package; 3 leads	SOT23

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#) and [Section 9](#)).

### 4. Marking

Table 5: Marking codes

Type number	Marking code <sup>[1]</sup>
PDTB113EK	E4
PDTB113ES	B113ES
PDTB113ET	*7U

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

### 5. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter	-	-50	V
$V_{CEO}$	collector-emitter voltage	open base	-	-50	V
$V_{EBO}$	emitter-base voltage	open collector	-	-10	V
$V_I$	input voltage				
	positive		-	+10	V
	negative		-	-10	V
$I_O$	output current (DC)		-	-500	mA
$P_{tot}$	total power dissipation		$T_{amb} \leq 25\text{ }^\circ\text{C}$		
	SOT346		<sup>[1]</sup> -	250	mW
	SOT54		<sup>[1]</sup> -	500	mW
	SOT23		<sup>[1]</sup> -	250	mW
$T_{stg}$	storage temperature		-65	+150	$^\circ\text{C}$
$T_j$	junction temperature		-	150	$^\circ\text{C}$
$T_{amb}$	ambient temperature		-65	+150	$^\circ\text{C}$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

## 6. Thermal characteristics

**Table 7: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]			
	SOT346		-	-	500	K/W
	SOT54		-	-	250	K/W
	SOT23		-	-	500	K/W

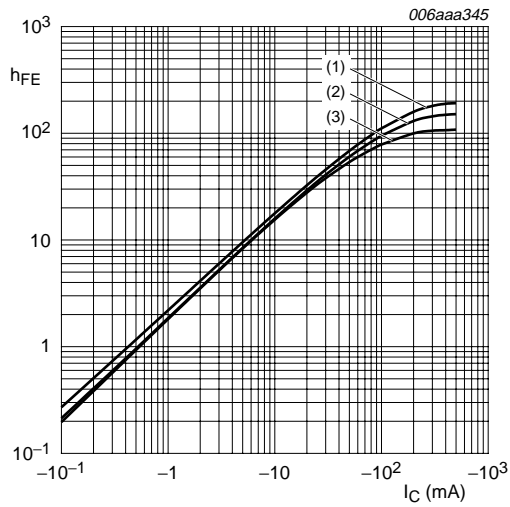
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

## 7. Characteristics

**Table 8: Characteristics**

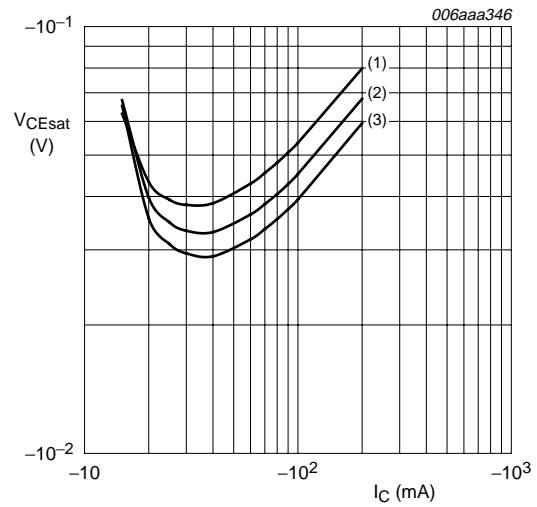
$T_{amb} = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -40\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
		$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = -50\text{ V}; I_B = 0\text{ A}$	-	-	-0.5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-4.0	mA
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -50\text{ mA}$	33	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -50\text{ mA}; I_B = -2.5\text{ mA}$	-	-	-0.3	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}; I_C = -100\text{ }\mu\text{A}$	-0.6	-1.1	-1.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}; I_C = -20\text{ mA}$	-1.0	-1.4	-1.8	V
R1	bias resistor 1 (input)		0.7	1.0	1.3	k $\Omega$
R2/R1	bias resistor ratio		0.9	1.0	1.1	
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 100\text{ MHz}$	-	11	-	pF



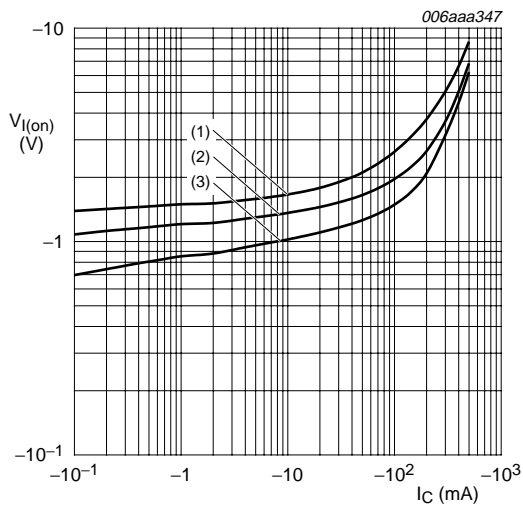
$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig 1. DC current gain as a function of collector current; typical values**



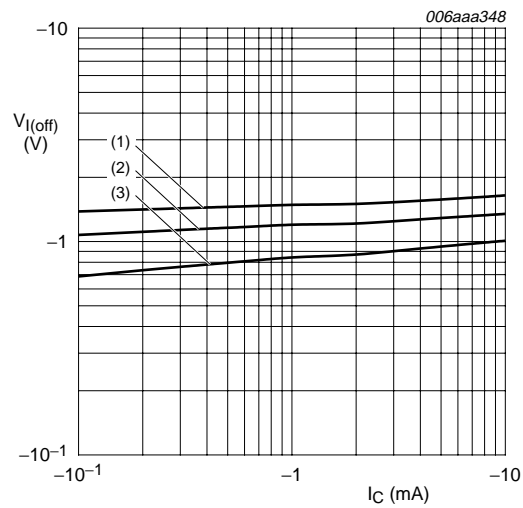
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = -0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

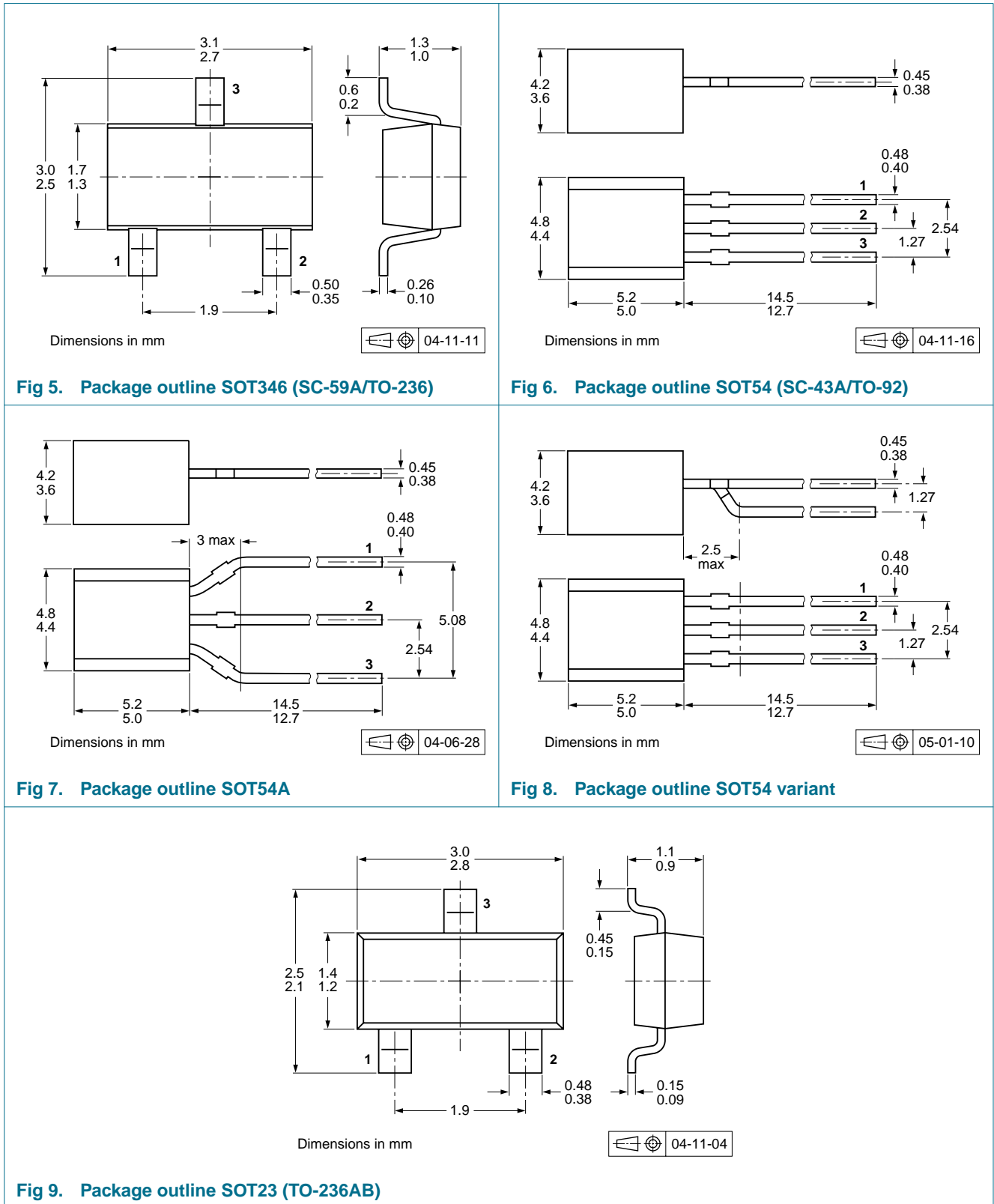
**Fig 3. On-state input voltage as a function of collector current; typical values**



$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig 4. Off-state input voltage as a function of collector current; typical values**

8. Package outline



## 9. Packing information

**Table 9: Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTB113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTB113ES	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
		tape ammopack, wide pitch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTB113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235

[1] For further information and the availability of packing methods, see [Section 14](#).

## 10. Revision history

**Table 10: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PDTB113E_SER_1	20050427	Product data sheet	-	9397 750 14902	-



## 11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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